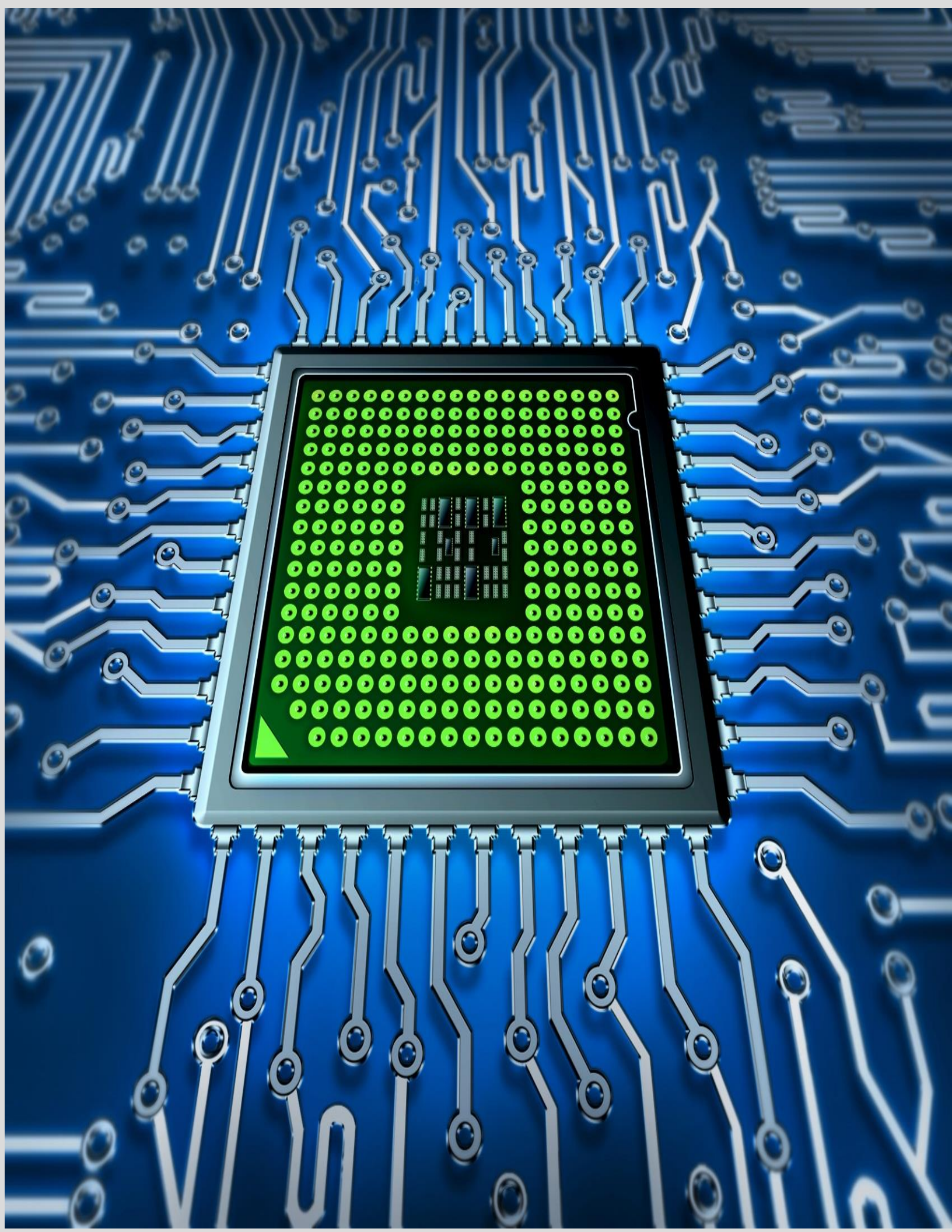


Created by

ARSLAN AHMED SHAAD (1163135)

MUHMMAD BILAL (1163122)

VISIT: www.vbforstudent.tk

Chapter # 3

Hardware specifications of 8086/8088

Short Questions:

What is meant by LATCH?

Latch is a D- type flip-flop used as a temporary storage device controlled by a timing signal, which can store 0 or 1.

What is the need for timing diagram?

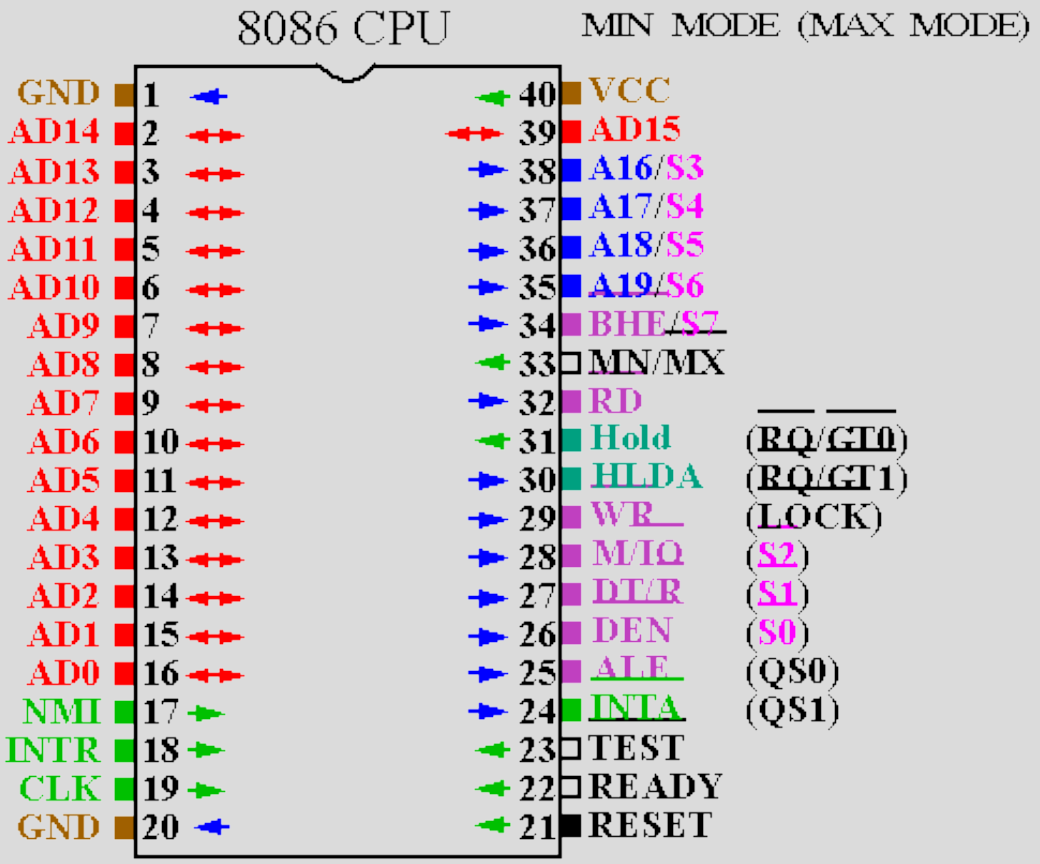
The timing diagram provides information regarding the status of various signals, when a machine cycle is executed.

Define T-State

T-State is defined as one subdivision of the operation performed in one clock period. These subdivisions are internal states synchronized with the system clock, and each T-State is precisely equal to one clock period.

Course Outline Questions:

Draw the pin diagram of 8086/8088



Explain the function of each pin?

Out of 40 pins, 32 pins are having same function in minimum or maximum mode, and remaining 8 pins are having different functions in minimum and maximum mode.

Following are the pins which are having same functions

$AD_0 - AD_{15}$

The 8080 address/ data bus lines composed the multiplexed address data bus. When ALE is logic 1 these pin will work as address bus, when ALE is logic 0 these pin will work as data bus. $AD_0 - AD_7$ carries low order byte data $AD_8 - AD_{15}$ carries higher byte data

A16/S3 – A19/S6

These are 4 address / status buses. During the first clock cycle it carries 4 bit address and later it carries status signal.

BHE / S7

It is used to indicate the transfer of data using data bus D_8-D_{15}. This signal is low during the first clock cycle, thereafter it is active.

INTR

It is used to request a hardware interrupt.

TEST

The test pin is an input that is tested by the wait instruction. When this signal is high the processor has to wait for the idle state, else the execution continues.

NMI

It stand for non maskable interrupt. It is an edge triggered input, which cause an interrupt request to the microprocessor.

RESET

The reset input cause the microprocessor to reset itself. This signal is active high for the first 4 cycle to reset the microprocessor.

CLK (clock)

It provides timing to the processor for operation.

READY

It is an acknowledgment signal from I/O devices that data is transferred. It is an active high signal. When it is high it indicates that the device is ready to transfer data, when it is low it indicates wait state

RD (read)

The read strobe indicates that the processor is performing a memory or I/O read cycle.

Mx / $\overline{Mn}$

It indicate that what mode the processor is to operate in. when it is high it works in minimum mode and vice versa.

MAXIMUM MODE PINS

QS0 – QS1

These are queue status signal and these signals provide the status of instruction queue.

S0, S1, S2

The status bit indicates the function of current bus cycle.

LOCK

The lock output is used to lock peripheral devices off the system. It indicates to the other processor not to ask the CPU to leave the system bus.

RQ/GT1 – RQ/GT0

These are the request grant signals used by the other processor requesting the CPU to leave the system bus.

MINIMUM MODE PINS

INTA

It is an interrupt acknowledgement signal when microprocessor receive this signal it acknowledge the interrupt.

ALE

Address latch enable indicates the availability of valid address / data lines

DEN

Data enable activates external data bus buffer.

DT/R

The data transmit / receive signal shows that the microprocessor data bus is transmitting or receiving. When it is high data is transmitted out and vice versa.

M / IO

This signal is used to distinguish between memory and I/O operations. When it is high it indicates I/O operation and when it is low it indicates the memory operation.

WR

This write signal is used to write the data into the memory or the output device depending on the status of M / IO signal.

HLDA

It stand for hold acknowledge signal and this signal acknowledge the hold signal.

HOLD

The hold input request a direct memory access.

Define and explain Maximum mode operation of 8086/88?

- In the maximum mode, the 8086 is operated by strapping the MN/MX pin to ground.
- In this mode, the processor derives the status signal S2, S1, S0. Another chip called bus controller derives the control signal using this status information.
- In the maximum mode, there may be more than one microprocessor in the system configuration. The components in the system are same as in the minimum mode system.

Define and explain Minimum mode operation of 8086/88?

- The microprocessor 8086 is operated in minimum mode by strapping its MN/MX pin to logic 1.
- In this mode, all the control signals are given out by the microprocessor chip itself. There is a single microprocessor in the minimum mode system.
- The remaining components in the system are latches, transceivers, clock generator, memory and I/O devices.

Sketch the pin diagram of Clock generator (8284A)?

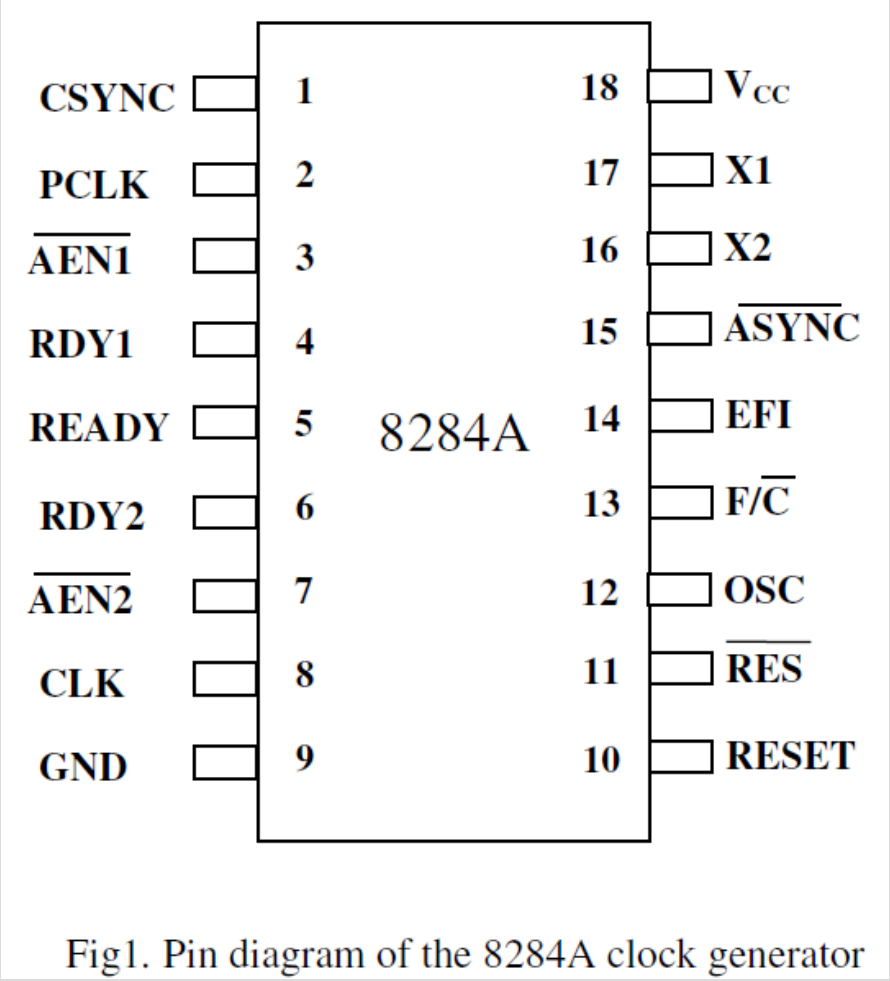


Fig1. Pin diagram of the 8284A clock generator

Explain the function of Clock generator (8284A)?

The 8284A is an ancillary component to the 8086/8088 microprocessor. Without the clock generator, many additional circuits are required to generate the clock (CLK) in an 8086/8088 based system.

The clock Generator 8284A provides the following basic functions or signals:

- clock generation
- RESEST synchronization
- READY synchronization
- TTL level peripheral clock signal.

Explain READY and WAIT state?

READY state:

The process is waiting to be assigned to a processor. Ready processes are waiting to have the processor allocated to them by the operating system so that they can run. Process may come into this state after Start state or while running it by but interrupted by the scheduler to assign CPU to some other process.

WAIT state:

A wait state is a situation in which a computer program or processor is waiting for the completion of some event before resuming activity. A program or process in a wait state is inactive for the duration of the wait state.

Describe Bus buffering and latching in 8086/88?

Bus Buffering:

A buffer allows a signal to drive more inputs than it would by itself, or provides input protection / amplification. For the 8086, it's used in the output sense, allowing internal signals to be made robust to drive external devices. Buffers pass an input through to output after some propagation time, possibly increasing drive strength (increasing fan-out).

Bus latching:

A latch is a circuit to accept and store one or more bits, with a 1-to-1 input / output ratio. Latches are used with 8086s to store addresses and data, and are used instead of registers because they maximize setup times. Latches additionally add memory, to capture and persist the input value at some point in time (memory). This latching behavior is triggered by a third signal, control.

Why we need bus buffering and latching in microprocessor?

Buffers are used in the output sense, allowing internal signals to be made robust to drive external devices.

Latches are used with 8086s to store addresses and data, and are used instead of registers because they maximize setup times

Explain Bus Timing?

This section provides insight into the operation of the bus signals and the basic read and write timing of the 8086/8088. It is important to note that we discuss only the times that affect memory and I/O interfacing in this section.

Explain how control signals MEMR, MEMW and I/ OW can be produced from the 8086/88 IO/M, RD and, WR/ control signals?

Using M/IO and DR/R lines, the 8086 signals which type of bus cycle is in progress and in which direction data are to be transferred over bus. The signal READ and WRITE indicates that a read bus cycle or a write bus cycle is in progress. The 8086 switches WR to logic 0 to signal external device that valid write or output data are on the bus.