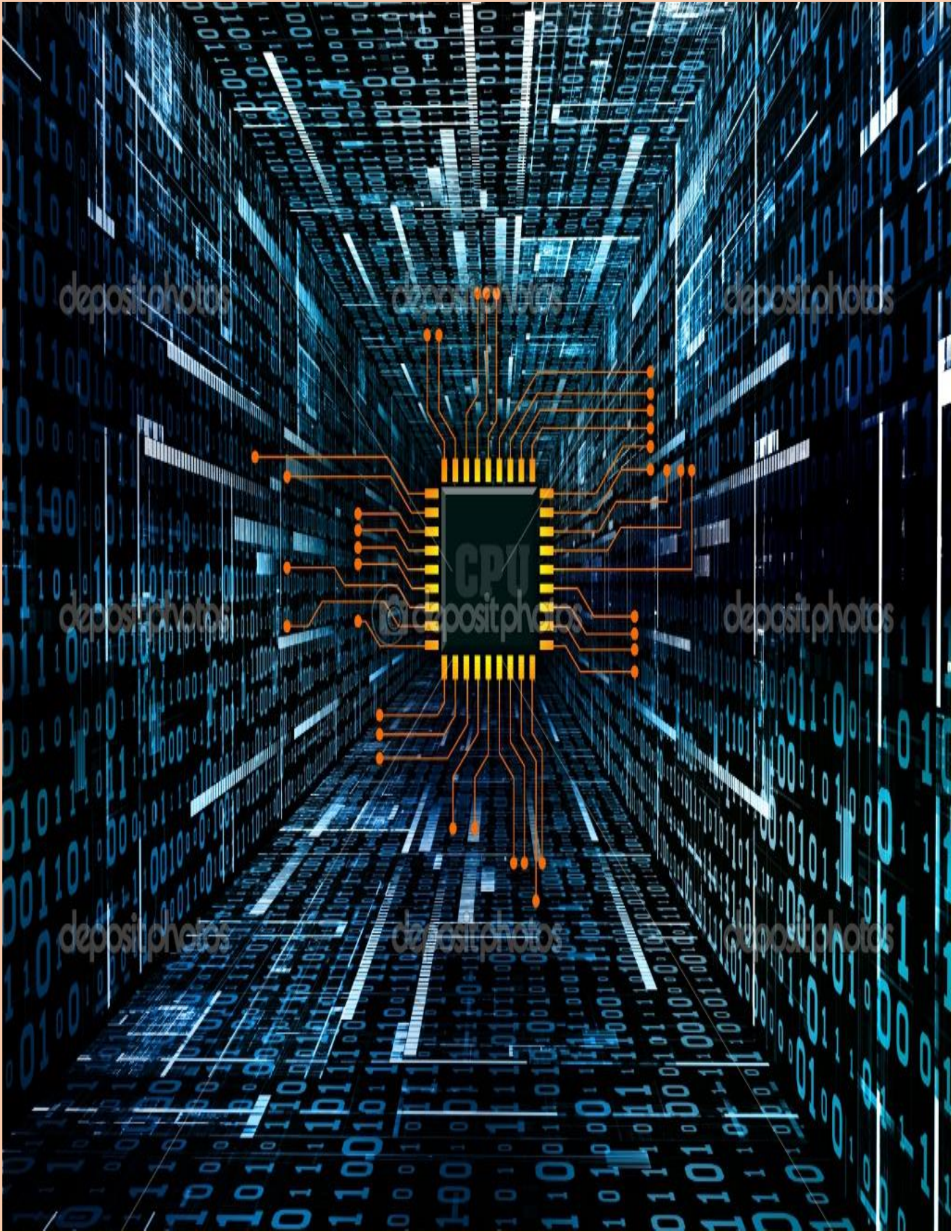
CPU

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For more notes of DAE

CHAPTER #6

Intel 8088/86 System Timing and Bus Multiplexing

COURSE OUTLINE QUESTION

Qno1 Define the following term?

T-State:

T-State is defined as one subdivision of the operation performed in one clock period. These subdivisions are internal states synchronized with the system clock, and each T-State is precisely equal to one clock period

Machine cycle:

The machine cycle is a 4 process cycle that includes reading and interpreting the machine language, executing the code and then storing that code.
Four steps of Machine cycle

Fetch - Retrieve an instruction from the memory.

Decode - Translate the retrieved instruction into a series of computer commands.

Execute - Execute the computer commands.

Store - Send and write the results back in memory.

Instruction cycle:

An instruction cycle (also known as the fetch–decode–execute cycle or the fetch-execute cycle) is the basic operational process of a computer. It is the process by which a computer retrieves a program instruction from its memory, determines what actions the instruction dictates, and carries out those actions.
This cycle is repeated continuously by a computer's central processing unit (CPU), from boot-up to when the computer is shut down.

Opcode fetch:

The duration in which microprocessor fetch the instruction frame memory into microprocessor is called opcode fetch

Or

The purpose of an OFMC is to read the contents of a memory location containing the opcode addressed by the program counter and to place it in the instruction register (IR).

Memory read cycle:

This is the total duration in which microprocessor read data from the given location of memory. For 8086/88 four T state (T1, T2, T3, T4) are required to read data from memory.
The following steps have to be followed in a typical read cycle:

1. Place the address of the location to be read on the address bus.
2. Activate the memory read control signal on the control bus.
3. Wait for the memory to retrieve the data from the address memory location.
4. Read the data from the data bus.
5. Drop the memory read control signal to terminate the read cycle.

Memory write cycle:

This is the total duration in which microprocessor write data into memory. The 8086/88 uses four T state to write data.
The following steps have to be followed in a typical write cycle:

1. Place the address of the location to be written on the address bus.
2. Place the data to be written on the data bus.
3. Activate the memory write control signal on the control bus.
4. Wait for the memory to store the data at the address location.
5. Drop the memory write control signal to terminate the write cycle.

I/O Read cycle:

This is the total duration in which microprocessor read data from the given input port. For 8086/88 four T state (T1 ,T2 ,T3, T4) are required to read data from input port.

I/O Write cycle:

This is the total duration in which microprocessor write data into output port. For 8086/88 four T state (T1 ,T2 ,T3, T4) are required to write data into output.

Qno2 Explain how the 8086/88 instruction decoder/machine cycle encoder produce suitable machine cycle in correct succession to produce a required instruction cycle?

Required instruction cycle:

Instruction decoding is a process in which binary code of assembly language is grouped into some specific part of instruction to perform given action according to the instruction.

The most common instruction consist of opcode, direction, width, more registers and memory bits. When these bits are applied on to their related circuits different types of signal and buses are generated.

In T1 : the address bus is setup, ALE =1, DEN 1, m/I, for memory m/I =1 for I/O m/I =1 signal are generated.

In T2 : the data bus is loaded with data bits ALE = 0, DEN =0 for read RD=0 for write WR = 0

Note T2: system check ready signal. If ready = 0 the tw (wait state)is instead if ready = 1 the system produce to T3.

In T3 : system will read data if RD=0 or the system will write data if WR = 0.

In T4 : the instruction execution is complete and system reset and ready for next operation.

In this way a complete instruction cycle which schedule opcode fetch and execution cycle take place.

Qno3 Explain interpret Timing Diagram for Common 8088/86 Instructions?

The common instruction of 8086/88 are as following

1: memory read cycle

2: memory write cycle

3: I/O read cycle

4: I/O write cycle

The timing diagram of 8086/88 consist of four time state (T1, T2, T3, T4)each timing state is used to perform save specific task during time period e.g.

In T1 : the address bus is setup, ALE =1, DEN 1, m/I, for memory m/I =1 for I/O m/I =1 signal are generated.

In T2 : the data bus is loaded with data bits ALE=0, DEN=0 for read RD=0 for write WR = 0

Note T2: system check ready signal. If ready = 0 the tw (wait state) is instead if ready = 1 the system produce to T3.

In T3 : system will read data if RD=0 or the system will write data if WR = 0.

In T4 : the instruction execution is complete and system reset and ready for next operation

In this way a complete instruction cycle which schedule opcode fetch and execution cycle take place.
In case or interrupt the microprocessor execute the current instruction. The microprocessor will send INTA signal to interrupting device, microprocessor will run interrupting service produced and provide service the microprocessor instruction.

Qno4 describe the purpose and implementation of the 8088/86 Wait, Halt and Hold states?

Wait :

The TW (wait state) is used for slow and fast I/O device to synchronize the timing with microprocessor.

Halt :

The meaning of halt is to stop the working of microprocessor. HLT command is used at the top of program.
A reset or an interrupt is required to get out from HLT process.

Hold :

The HOLD is the pin of 86/88. This pin is connected with DMA. During HOLD condition microprocessor handers us to DMA and discount itself from main memory. When DMA disable the hold state the microprocessor again takeover the system buses and start working normally.

BEST OF LUCK