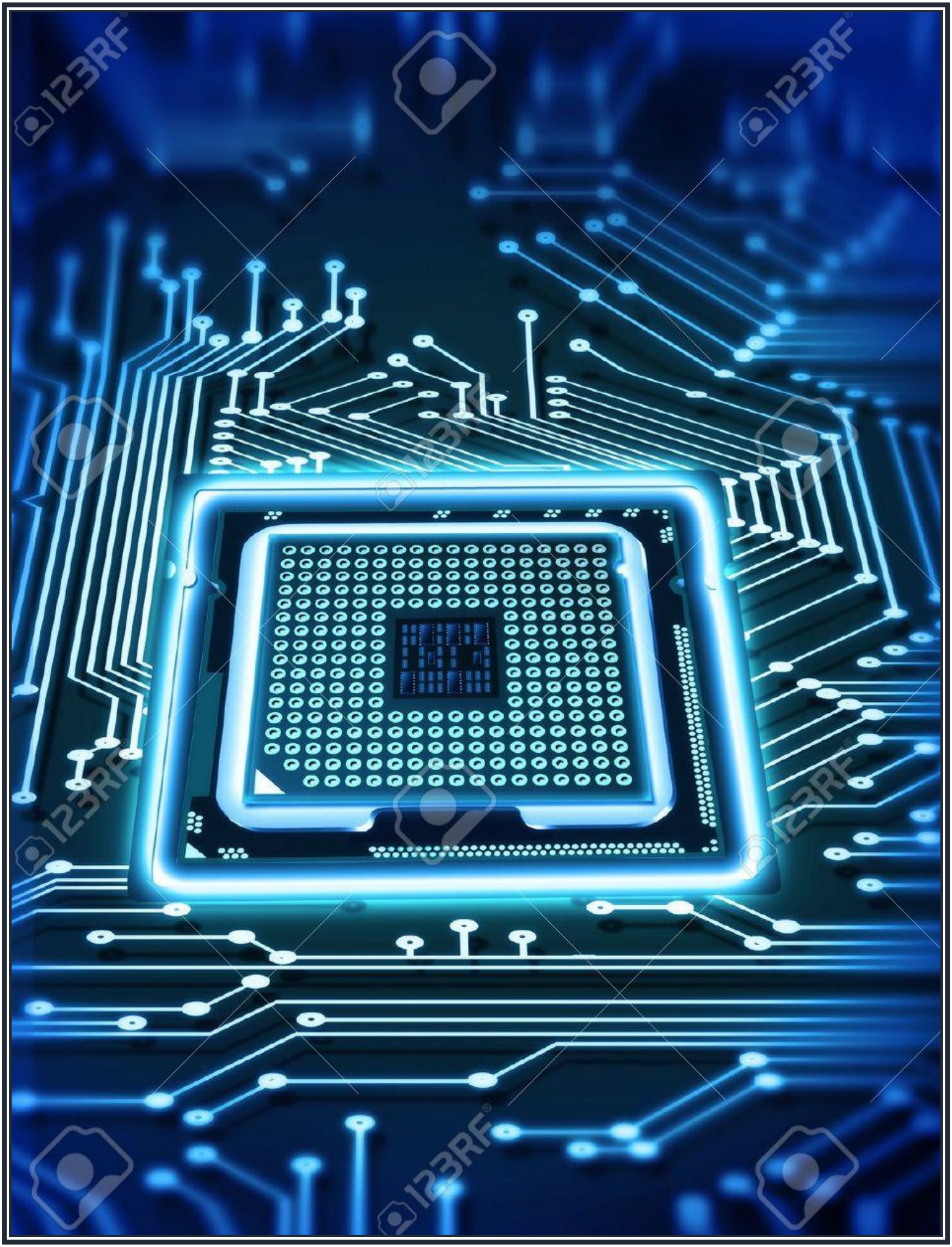

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CHAPTER # 7

Interfacing to Intel 8088/86

COURSE OUTLINE QUESTIONS

Qno1 Explain the different terms of interfacing?

Isolated I/O

When addressing I/O devices dedicatedly without memory mapping is called isolated I/O. In the isolated I/O scheme, the IN, INS, OUT, and OUTS instructions transfer data between the microprocessor's accumulator or memory and the I/O device. A disadvantage of isolated I/O is that the data transferred between I/O and the microprocessor must be accessed by the IN, INS, OUT, and OUTS instructions. Separate control signals for the I/O space are developed (using and), which indicate an I/O read ( ) or an I/O write ( ) operation

Memory Mapped I/O

Memory-mapped I/O does not use the IN, INS, OUT, or OUTS instructions. Instead, it uses any instruction that transfers data between the microprocessor and memory. A memory-mapped I/O device is treated as a memory location in the memory map. The main advantage of memory-mapped I/O is that any memory transfer instruction can be used to access the I/O device.

Unconditional I/O

The method used to provide services to connected I/O devices without any hand shaking signals is called unconditional I/O e.g. monitor

Polled I/O

When microprocessor provide regular service with some specific interval of time to all devices is called polled I/O. the main disadvantage of this technique is that I/O devices cannot provided with priority services.

Interrupt Service Routine

ISR Stands for "Interrupt Service Routine." An ISR (also called an interrupt handler) is a software process invoked by an interrupt request from a hardware device. It handles the request and sends it to the CPU, interrupting the active process. When the ISR is complete, the process is resumed.

A basic example of an ISR is a routine that handles keyboard events, such as pressing or releasing a key. Each time a key is pressed, the ISR processes the input.

Interrupt Vector

An interrupt vector is a 4-byte number stored in the first 1024 bytes of the memory (00000H–003FFH) when the microprocessor operates in the real mode. In the protected mode, the vector table is replaced by an interrupt descriptor table that uses 8-byte descriptors to describe each of the interrupts. Each vector interrupt consist four bytes. First two bytes are used to hold IP offset address and other two bytes hold segment address.

Service Request Flag

The signal send to I/O device from DMA to tell to start requested service that signal called service request flag.

Strobed Port

All I/O ports used to input/output data basis of hand shaking signals are called strobed ports.

Qno2 Explain Absolute Address and Linear Address Decoding?

Absolute address decoding

The decoding in which all available address line (16 lines in memory mapped and 8 lines in peripheral mapping) are used for decoding to generate a unique address is called absolute decoding

Linear address decoding

The decoding in which all available address line (16 lines in memory mapping and 8 lines in peripheral mapping) are not used for decoding resulting in multiple address for same port is called partial decoding or linear decoding.

Qno3 Explain Programmable interval timer (8254)?

The 8254 programmable interval timer consists of three independent 16-bit programmable counters (timers). Each counter is capable of counting in binary or binary-coded decimal (BCD). The maximum allowable input frequency to any counter is 10 MHz This device is useful wherever the microprocessor must control real-time events. Some examples of usage include real-time clock and an event counter, and for motor speed and direction control.

Qno4 Explain Programmable Peripheral Interface (PPI).

The 82C55 programmable peripheral interface (PPI) is a very popular, low-cost interfacing component found in many applications. The PPI, which has 24 pins for I/O that are programmable in groups of 12 pins, has groups that operate in three distinct modes of operation. It is used to interface to the keyboard and a parallel printer port in PCs (usually as part of an integrated chipset).

Qno5 Describe Priority Interrupt control unit in 8086/88 based system?

For applications where we have interrupts from multiple source, we use an external device called a priority interrupt controller (PIC) to the interrupt signals into a single interrupt input on the processor. The Programmable Interrupt Controller (PlC) functions as an overall manager in an Interrupt-Driven system. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination

Qno6 Describe Basic I/O interface?

An Input-Output (I/O) interface is the piece of equipment or location at which information can be input and output from a device such as a computer. The basic input device is a set of three-state buffers. The basic output device is a set of data latches. The term IN refers to moving data from the I/O device into the microprocessor and the term OUT refers to moving data out of the microprocessor to the I/O device. Whenever data are transferred by using the IN or OUT instructions, the I/O address, often called a port number (or simply port), appears on the address bus. The external I/O interface decodes the port number in the same manner that it decodes a memory address.

Qno7 What is Direct Memory Access (DMA)?

Direct memory access (DMA) is a method that allows an input/output (I/O) device to send or receive data directly to or from the main memory, bypassing the CPU to speed up memory operations. The process is managed by a chip known as a DMA controller (DMAC). The DMA transfer speed can approach 33 to 150 M-byte transfer rates with today's high-speed RAM memory components.

BEST OF LUCK